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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,813	01/27/2004	Lakshmanan Ramakrishnan	15142US02	2449

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EXAMINER	
WERNER, DAVID N	

ART UNIT	PAPER NUMBER
2621	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,813	RAMAKRISHNAN, LAKSHMANAN	
	Examiner	Art Unit	
	David N. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action for US Patent Application 10/765,813 is in response to communications filed 17 June 2008, in reply to the Non-Final Rejection of 13 March 2008. Currently, claims 9-12 and 20 are pending. Claims 1-8 and 13-19 have been cancelled.

2. In the previous Office action, claims 9-12 and 20 were rejected under 35 U.S.C. 102(e) as anticipated by US Patent 7,007,031 B2 (MacInnis et al.), which shares assignee with the present invention, and claims 5, 7, 8, and 16-19 were rejected under 35 U.S.C. 103(a) as obvious over US Patent 6,178,203 B1 (Lempel) in view of US Patent 4,599,689 (Berman). The title of the invention was objected to as non-descriptive.

Response to Arguments

3. Applicant's arguments filed 17 June 2008 have been fully considered but they are not persuasive. Applicant argues that the command from a core processor to a bridge module to fetch data from a main memory to a data unit processing pipeline in MacInnis et al. (column 6: lines 10-14) when a buffer memory in the data processing pipeline is free (column 11: line 63–column 12: line 7) is not the claimed "indicator...indicating that the local buffer can store another potion of the video data". MacInnis et al. operates on a five-stage pipeline (column 10: lines 10-27). In the first five clock cycles, the pipeline components operate on data within buffer 400 (column 10: line 28–column 11: line 62).

In the fifth stage of the pipeline, bridge module 204 transfers the data in the buffer out of the pipeline (column 11: lines 41-47). Only once the buffer is cleared may new data be loaded (column 11: lines 63-65). Then, since this buffer is part of decoder memory 212 addressed by core processor 202 (column 6: line 64–column 7: line 2), the instruction from core processor 202 to fetch data from main memory 110 to decoder memory 212 via bridge module 204 (column 6: lines 10-14, 46-51), it is inherent to the proper operation of the MacInnis et al. device that the fetch command from core processor 202 is may be executed ONLY IF buffer 400 in memory 212 is free. Therefore, a valid data fetch command MUST indicate that the buffer is open and ready to store additional data, to prevent data collision in the pipelined processor. See Hamacher et al., *Computer Organization*, pp. 302-311 for a further illustration on data flow within a pipelined system. Note that if an instruction is unable to be immediately performed due to a dependency on unavailable data, busy status of a component, memory delay time, flushing instructions due to a branch, &c, the instruction is delayed until all conditions are satisfied. Therefore, the examiner respectfully maintains the rejections based on MacInnis et al.

Specification

4. **The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. If this deficiency has been corrected in response to a previous Office action and**

overlooked by the Examiner, Applicant's assistance in showing where in the correspondence with the Office this occurred is greatly appreciated.

The following title is suggested: "Automatic Direct Memory Access Engine and Method for Dual Macroblock Row Transfer in a Video Decoder".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 7,007,031 B2 (MacInnis et al.).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

MacInnis et al. discloses a memory system and a pipeline for a video decoder. Regarding claim 9, figure 2 of MacInnis et al. illustrates a media decoding system that can be used as a video decoder (column 5: lines 20-22). Decoder memory 212 locally

stores a data unit containing macroblock information received from main memory (column 6: lines 1-14). This corresponds with the claimed "local buffer". When decoding system 200 acts as a video decoder, core processor 202, co-processor 206, and accelerators 208 and 210 comprise a chipset that performs picture decoding and decompressing (column 6: lines 15-20). Each component uses decoder memory 212 as a local memory (column 6: lines 52-64). Then, decoder 200 corresponds with the claimed "decompression engine". Bridge module 204 communicates with the local decoder memory 212 and main memory 110, according to instructions from core processor 202 (column 6: lines 46-51). This corresponds with the claimed "extractor". The bridge module acts to fetch data from main memory 110 into a pipelined data processing system including local decoder memory 212 (column 6: lines 4-14) when a buffer memory has output a previous macroblock and is free to receive additional data (column 11: line 63–column 12: line 7). Then, the fetch instruction, indicating that the buffer is open, corresponds with the claimed "indicator".

Regarding claim 10, as shown in figure 1 of MacInnis et al., DMA controller 106 controls data transfer between system memory 110 and a local memory in video decoder 116 (column 4: lines 57-64). Then, when core processor 202 in video decoder 116 issues a command to read from system memory 110 to local memory 212 through bridge module 204, it inherently does so through DMA controller 106.

Regarding claim 11, core processor 202 acts to direct a pipeline, individually receiving and processing macroblocks one at a time and storing them in local memory 212. The local memory, in turn, contains a plurality of buffers that each store

information for one macroblock between operations (column 7: lines 20-41). In the illustrative example described throughout MacInnis et al., five buffers each store macroblock data during processing. When a buffer becomes free, core processor 202 stores a new macroblock to continue decoding (column 16: lines 15-35).

Regarding claim 12, as mentioned previously, local memory 212 contains a plurality of buffers, each of which can store data for a different macroblock simultaneously, and co-processor 206 contains two separate units that can simultaneously decode different macroblocks (column 13: lines 26-35).

Regarding claim 20, digital media system 100 of MacInnis et al. corresponds with the claimed "decoder system", digital video decoder 116 corresponds with the claimed "video decoder", decoder memory 212 corresponds with the claimed "local buffer", bridge 204 corresponds with the claimed "extractor", and DMA controller 106 corresponds with the claimed "direct memory access engine".

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner whose telephone number is (571)272-9662. The examiner can normally be reached on Monday-Friday from 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/
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